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Flexible High-Speed CODEC Final Report Task 6

Greg P. Segallis, Jim V. Wernlund, and Glen Corry
Harris Corporation
Melbourne, Florida

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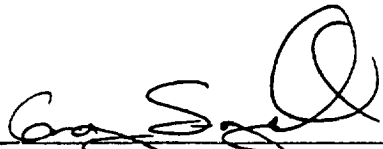
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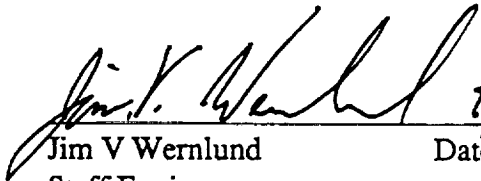
National Aeronautics and
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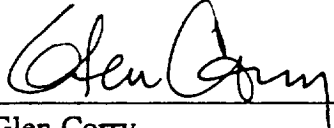
For NASA Lewis Research Center
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Greg P Segall
Lead Engineer

7/27/92
Date


Jim V Wernlund
Staff Engineer

7/28/92
Date


Glen Corry
Program Manager

7-27-92
Date



HARRIS

Harris Government Communication Systems Division

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1.0 SCOPE

This report is prepared by Harris Government Communication Systems Division for NASA Lewis Research Center under contract NAS3-25087. It is written in accordance with SOW section 4.0 (d) as detailed in section 2.6. The purpose of this document is to provide a summary of the program, performance results and analysis, and a technical assessment.

2.0 APPLICABLE DOCUMENTS

Task II Report
Task III report
Task IV report
TDE ATP - ESD 23412
BCH ATP - ESD 22580
HARRIS-NASA BCH ASIC Data Sheet

3.0 REQUIREMENTS

The purpose of this program was to develop a Flexible, High-Speed CODEC that provides substantial coding gain while maintaining bandwidth efficiency for use in both continuous and bursted data environments for a variety of applications. A key objective was to develop a highly integrated ASIC that would be suitable for use as a building block in various communications systems. The proposed Harris system consisted of implementing a hard decision, triple error correcting, block codec on an ASIC. A Bose-Chaudhuri-Hocquenhem (BCH) code was selected. It also included development of a Chase Algorithm, soft decision appliqué built around several of the BCH ASICs to further increase coding gain. Test and Demonstration Equipment (TDE) was also to be developed to verify and exercise the codecs.

Harris proposed a coding system consistent with the requirements specified in SOW section 3.1.1:

- (a) The BCH ASIC should provide up to 4 dB of coding gain. The soft decision appliqué, designated the FHSC, was to provide an additional 1.3 dB of coding gain using soft decision information. The code rate should range from 7/8 to 15/16.
- (b) The BCH and FHSC should operate at data rates up to 300 Mbps (information rate).
- (c) The BCH and FHSC should be compatible with QPSK, 8-PSK and 16-PSK modulation systems.

- (d) It should provide continuous or bursted modes of operation with bursts consisting of from 224 to infinity data bits in increments of 16.
- (e) The BCH should be able to switch from coded to uncoded at the encoder, decoder or both, on a block by block basis with no change in throughput delay.
- (f) The BCH should provide error location information to the Chase appliqué for soft decision operation.

The BCH should provide carrier phase ambiguity resolution for QPSK and 16-PSK modulation modes.

The FHSC should provide carrier phase ambiguity resolution for QPSK, 8-PSK and 16-PSK, hard decision only, modulation modes.

The interface to the chip should support single symbol widths of 2 or 4 bits as well as a multiple symbol width of 8 bits for maximum throughput.

The TDE should allow all modes of operation of both the BCH codec ASIC and the FHSC codec chassis to be exercised (using the FHSC to test certain modes of the BCH), providing all data interface, mode control, TDMA controller, and link simulation functions. This unit should be user configurable.

4.0 PERFORMANCE RESULTS

The performance results of the BCH & FHSC codecs as well as the TDE are provided here per SOW sections 3.1.1 and 3.1.2.

4.1 TDE Performance

The first function of the TDE chassis is to provide data formatting from a gated serial bit stream (a TX BERT) up to 343 Mbps and convert it to the selected interface format of either the BCH or FHSC codec, and provide the reverse operation from the codec to a gated serial bit stream. The TDE has been verified to provide this function error free at up to 114 Mbps with odd length PN data and up to 250 Mbps with even length PN data. The performance of the parallel to serial conversion circuitry (the output portion) on the I/O Formatter circuit card assembly (CCA) degrades to varying degrees at rates above this and at certain rates below this, and is also data dependent. There are several reasons this problem exists. This is addressed in the analysis section of this document along with the solution.

The second function of the TDE is to provide the mode control signals to the codecs as well as generate a specific burst sequence. This "profile" is under software control via an IBM compatible PC and allows all profile characteristics to be easily selected by the user. The burst sequence may consist of 1 to 4096 blocks of length 224 to 480 data bits, optionally followed by a single block of different length 224 to 480. The burst will then repeat after a gap of from 0 to 4096 bits (2,101,248 if the burst contains only 1 block). This function works as specified in all modes.

The third function is to provide a link channel simulator for QPSK, 8-PSK and 16-PSK modulation, introducing Additive White Gaussian Noise (AWGN) as well as a carrier phase ambiguity for various E_b/N_0 's, all under software control via the PC. The Digital Noise Generator was verified to perform within 0.1 dB of theory for all BCH modes up to 280 Mbps (although the I/O Formatter problem will not allow a BER measurement to be performed at this rate). These results are shown in figure 4.1.1. Performance concerns above 280 Mbps are addressed in the Analysis section.

Due to the descoping of the program, the FHSC chassis was not built. Therefore, many of the FHSC specific modes of the TDE have not been thoroughly tested.

Although the TDE failed to operate at 300 Mbps, all tested modes performed exactly as designed at lower speeds and all problem areas have been identified as well as their potential solutions. The outstanding performance of this noise generator is significant, allowing very accurate testing of the BCH ASIC. Error rates down to 10^{-10} along with complete programmability make this design applicable to many situations.

Noise Generator BER

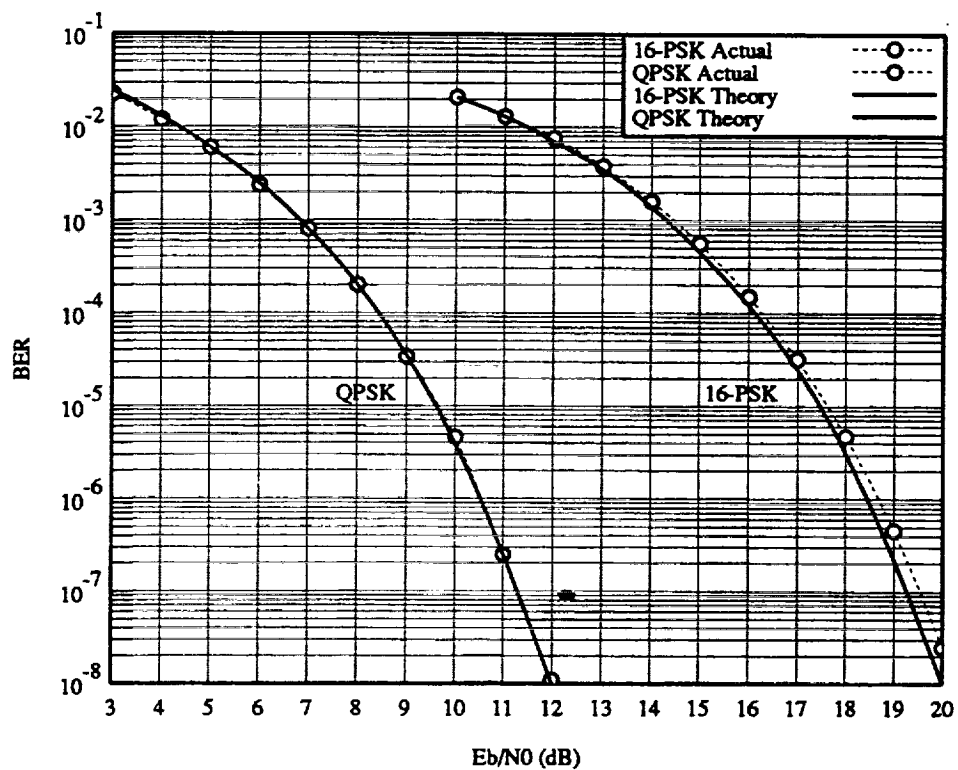


FIG 4.1.1 - Noise Generator BER Performance

4.2 BCH Performance

The BCH ASIC performance was verified for QPSK, single symbol, burst; 16-PSK, single symbol, burst; 16-PSK, 8-wide, burst; and 16-PSK, 8-wide, continuous modes. The BCH performed to within 0.1 dB of theory in each case. The block by block switching between coded and uncoded, variable block lengths, variable user bits, carrier phase ambiguity resolution, codeword position acquisition, and programmable lock thresholds were all verified to work exactly as designed. Due to the problems with the TDE I/O Formatter CCA, the BCH could only be tested at up to 114 Mbps for error free, odd length PN operation, and 250 Mbps for error free, even length operation. In addition the BCH was observed to lock up to the data at rates up to 300 Mbps, although no BER measurements could be made.

The BER performance is characterized in figures 4.2.1 and 4.2.2. Notice in both plots that the performance difference over the range of codeword lengths is reduced at lower bit error rates, as expected. Also, note that in the 16-PSK plot the deviation of the "Coded Actual" curves from the "Coded Theory" curve, as the bit error rate is reduced, is due to the fact that the "Uncoded Actual" curve diverges from the "Uncoded Theory" curve (i.e. the noise generator is actually off from theory). It is not due to reduced Codec performance. This is proved by observing that the coding gain from "Coded Theory" to "Uncoded Theory" is identical to the coding gain from "Coded Actual" to "Uncoded Actual".

The single symbol continuous modes for QPSK and 16-PSK (2 wide and 4 wide) exposed a system level anomaly within the BCH design. The two gated data clocks that come from the BCH encoder to clock data from the data source occur early. This problem exists because of the way the encoder generates its internal blockmark signal using the divided down, 16 wide internal clock (in burst mode the internal 16 wide clock is synched after blockmark). The result is that the data clock is gated "on" earlier than it should be. Since our TDE always expects that clock to occur at the same time, the first symbols worth of data clocked out by the TDE is ignored by the BCH. This is verified by measuring the BER which will show consistent errors at the block boundaries (a data shift). Also, since the data is corrupted upon entry to the encoder, the BCH decoder will lock up and operate as usual. This is verified by observing that the BER does not change from coded to uncoded, since there are actually no errors in the codeword. If the RX BERT is programmed to look for the TX BERT pattern with the leading and trailing bits altered accordingly, the BERT will show error free operation. All BCH lock operation is valid. The solution to this problem as well as possible system work arounds and a TDE work around are discussed in the analysis section.

The throughput delay of the TDE and BCH was measured to be 1002 bits (TX BERT to RX BERT). This delay remains constant while switching modes, as designed.

Aside from the clock anomaly explained above, all modes of the BCH performed exactly as designed. These results demonstrate the extensive versatility provided by the ASIC.

QPSK BER

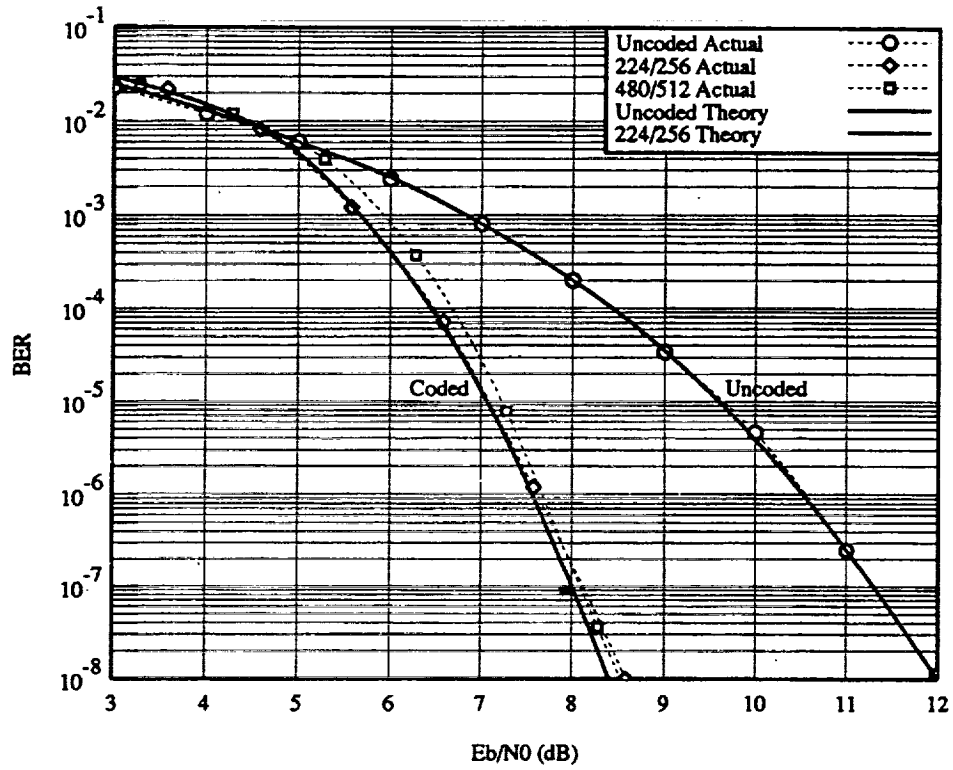


FIG 4.2.1 - BCH QPSK BER Performance

16-PSK BER

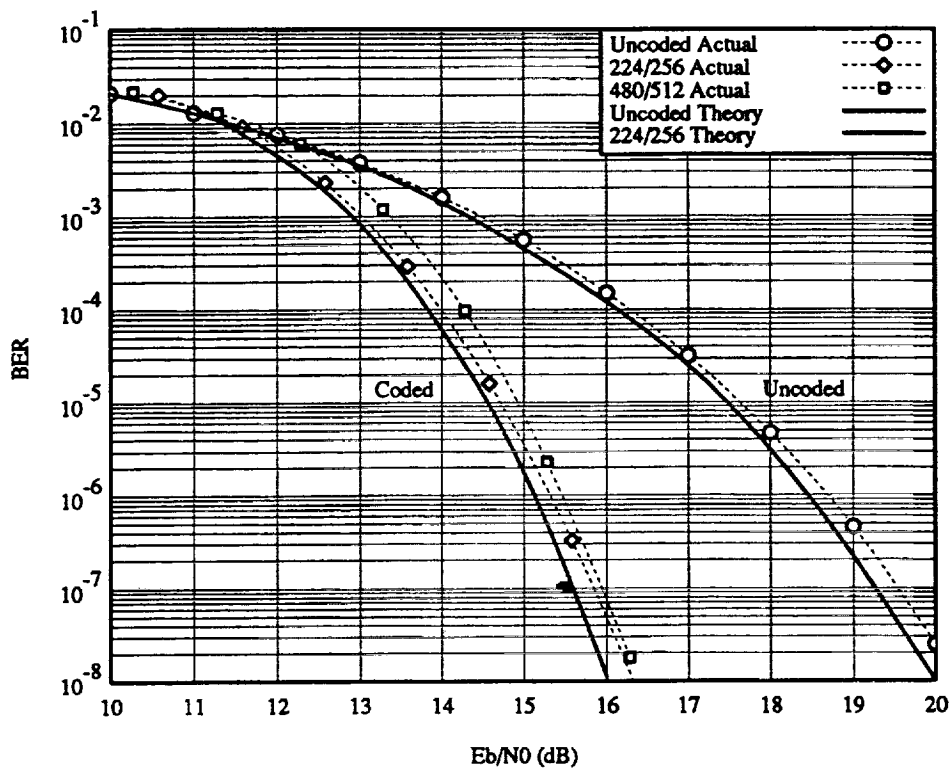


FIG 4.2.2 - BCH 16-PSK BER Performance

4.3 FHSC Performance

Due to the descoping of this program the FHSC chassis was not built. The design was completed and partially simulated. One CCA was completely simulated and wire wrapped. One CCA is 90% simulated and the remaining 2 CCA's are yet to be simulated. These results are included as appendix D of this report.

The TxFormatter card was completely simulated. This simulation verified the operation of the Tx 8-ary to nibble circuits, the nibble to word circuits, the word to nibble circuits and the nibble to 8-ary circuits. These circuits perform the input/output FIFO function needed to interface the users symbols to the ASIC. The timing diagrams demonstrate this function for QPSK, 8-ary and 16-ary modes of operation. This card was simulated at a functional level. That is, each function of the design was simulated stand alone.

The RxFormatter card has been 90% simulated. As with the TxFormatter, the simulations demonstrate the FIFO function between the USER and the ASIC. In both

designs, the control signals are slaved off of the user generated Block-Mark signal. Unlike the TxFormatter card the RxFormatter card was simulated by linking each of the schematic sheets together and letting the design function at a card level. This approach was found to be very thorough, although more difficult to debug.

The simulation effort proved to be very helpful in demonstrating the functions provided by the design and caught several subtle errors in the design. In particular it demonstrates the FIFO functions within the FHSC and its ability to handle arbitrary delays between the User and the FHSC chassis. These simulation results provide a potential solution to the problems the TDE experiences at high speeds.

The functions that remain to be simulated are the Hard and Soft Memory circuits, Pre and Post Log-Likelihood Calculator circuits and the Select Most Likely circuits.

5.0 TECHNICAL ANALYSIS

5.1 TDE Analysis

The TDE noise generator implements a clock doubler for 8 wide BCH interface widths. This doubler utilizes an active delay element and an exclusive-or gate to generate the twice rate clock. We have had problems with these delay elements meeting their specifications as well as problems setting their delay period. They also distort the signal and add quite a bit of noise. The result is that the clock doubler only runs up to about 300 Mbps currently. The clock doubler performance could be improved by replacing the delay element with a wire delay. We used lengths of twisted pair to provide delays in other areas of this design and it proved to be extremely accurate and much more effective than the active delay elements. This is a simple fix and has negligible risk.

The parallel to serial converter on the I/O Formatter CCA (IOFC) has several problems:

- (1) Similar problems with the active delay elements. With a minimum clock period of less than 3 ns it is easy for this problem to degrade performance at speed. The solution is to replace these active delay elements with wire delays.
- (2) Another problem that exists with the IOFC is the clock routing. Several critical high speed clock lines are fanned out to 5 loads. This creates a lot of distortion and noise on the clocks. We have determined that at these speeds, fanout should be limited to 2 loads on critical nodes.
- (3) During the initial checkout of this CCA, several modifications were incorporated utilizing mag wires. Signals at these speeds need to be matched transmission lines. These mag wires have added another element of unreliability.
- (4) The design of the BCH and FHSC codec is dependent on a blockmark signal. This signal is used throughout the codecs to synchronize events and generate control and gated clock signals. Due to the varying delay through subsystems, synchronization must be restored. That is what the blockmark signal is used for. The TDE design, however, attempts to synchronize events by using active delay elements to match the subsystem delays. The problem is that as the clock speed increases the delay becomes longer than the clock period. This causes "dead spots" in the performance at certain data rates as the clock edges approach alignment with each other. This is an unreliable and more complicated approach to the problem.

The solution to items (2) - (4) is to redesign the identified areas of the IOFC, utilizing the blockmark signal for synchronization, and re-layout the board reducing fanout and using striplines.

5.2 BCH Analysis

The only problem with the BCH is that the two gated data clocks that come from the BCH encoder to clock data from the data source are early. These clocks occur early due the way the BCH uses a divide-by-16 clock to generate blockmark. This anomaly can be bypassed by either regenerating the data clock, delaying the data via a register, or by using blockmark-out to gate the data itself. The data into the BCH is in no way corrupted, rather the first two symbols provided by the data source are ignored by the BCH encoder. If the ASIC were redesigned for another reason, a modification could be made to solve the problem. This only affects the continuous mode and only if the single symbol interface is selected. The ASIC is fully functional and while this clock data timing is not as desired, it is completely useable.

5.3 FHSC Analysis

Simulations indicate the design is sound. In particular they demonstrate the FHSC 's tolerance to delays between the User and FHSC. Completion of this effort would significantly reduce risk if this chassis is built. Clock rates within the FHSC chassis never exceed 120 Mhz and the FIFO's of the FHSC ensure that arbitrary delay is not a problem. Based on the simulation results, we believe this design will meet all of its design goals.

6.0 ASSESSMENT

The BCH codec is adaptable to many applications. The high coding gain and code rate are extremely valuable. The high data rate capability lends itself well to state of the art systems. These key features in a small, low power package give the BCH great potential for use. Significant interest in the BCH from various sources has been expressed. Harris, on behalf of Harris and NASA, is pursuing a patent on part of the BCH ASIC design, as well as seeking applications for its use.

The TDE Noise Generator provides a sophisticated test capability. The digital implementation allows for accurate, versatile, and repeatable test conditions. This design could be reused easily in the future by NASA.

The FHSC is ready for final simulation and then fabrication. This would provide NASA with two soft decision codecs capable of being easily interfaced to a NASA modem and allowing actual system level operation. Harris would like the opportunity to implement the FHSC chassis, and so demonstrate the Chase algorithm performance.

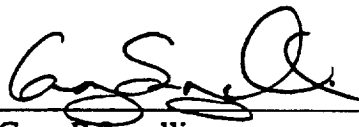
7.0 APPENDICIES

- A TDE ATP with test results**
- B BCH ATP with test results**
- C BCH Data Sheet**
- D FHSC Simulation Data**


APPENDIX A

FHSC TDE Acceptance Test Procedure

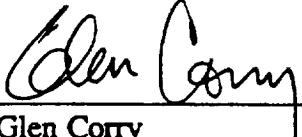
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Glen Corry
Program Manager

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Robert Jones
NASA LeRC



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Harris Government Communication Systems Division

ESD 23412

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NOTE: ACTUAL TEST RESULTS ARE UNDERLINED ITALICS

1.0 Scope

This document describes the tests necessary to verify proper operation of the FHSC Test and Demonstration Equipment (TDE). The DC tests validate the power supplies and reference voltages. AC tests validate the chassis IO and Block Profiles. The Performance tests validate the Noise Generator Circuits.

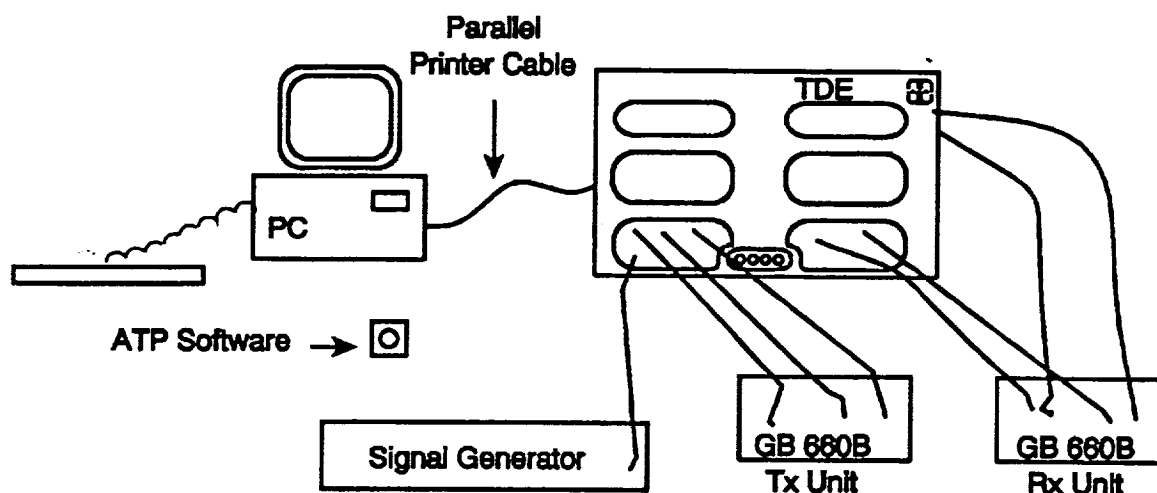


Fig 1

2.0 Applicable Documents

ESD 22581 BCH Specification
Assy- 17967 TDE Chassis Assembly
Assy- 179704 BCH Card Assembly
ATP Software

3.0 Required Test Equipment

Model	Description	S/N	Cal Due
WaveTek 3510	Signal Generator	<u>150154</u>	<u>9/92</u>
O-Scope	Tektronix 485	<u>150873</u>	<u>9/92</u>
Hp 5334A	Counter/ DVM		
1630G	Hp Logic Analyzer	<u>150389</u>	<u>10/92</u>
Tx660B	uWave Logic Data Generator	<u>134450</u>	
Rx660B	uWave Logic Error Detector	<u>134451</u>	
T-TBD	Converter box (#TBD)	<u>001</u>	

4.0 Specifications

4.1 Power Supply

The tests shall be performed with :

$V_{cc} = +5.0 \text{ Volts} \pm 0.25 \text{ Volts}$

$V_{tt} = -2.0 \text{ Volts} \pm 0.10 \text{ Volts}$

$V_{ee1} = -4.5 \text{ Volts} \pm 0.20 \text{ Volts}$

$V_{ee2} = -5.2 \text{ Volts} \pm 0.25 \text{ Volts}$

4.2 Environment

The tests shall be performed at $25^{\circ} \text{C} \pm 5^{\circ} \text{C}$

5.0 Test Procedure

5.1 Purpose

The purpose of the following tests is to verify proper electrical characteristics, functional performance and operational performance of the FHSC test and Demonstration Equipment.

5.2 DC testing.

5.2.1 DC Power Supplies

The following test verifies the DC voltages with in the TDE chassis. Turn on TDE and verify the front panel voltage indicator lights light up

+5.0 Volts	<u>OK</u>
-2.0 Volts	<u>OK</u>
-4.5 Volts	<u>OK</u>
-5.2 Volts	<u>OK</u>

With the bottom cover off measure the DC voltages at the card cage

+5.0 Volts	<u>5.04</u>
-2.0 Volts	<u>-2.06</u>
-4.5 Volts	<u>-4.56</u>
-5.2 Volts	<u>-5.20</u>

5.2.2 Reference Voltage

The following test verifies the reference voltages Ref1 and Ref2 on the back panel. These are used to bias the complementary inputs of the Rx BERT. On the back panel measure the voltages Ref1 and Ref2. Nominally these voltages should be -1.3 Volts. Use a "T" adapter as the references are open emitter outputs and must therefore be terminated to -2V.

-1.2 > Ref1 > -1.4 Volts	<u>-1.288</u>
-1.2 > Ref2 > -1.4 Volts	<u>-1.296</u>

5.3 AC Performance Testing

5.3.1 Interfaces

The following test validate the Clocks, Data and Block Mark signals out of the TDE chassis. With the Signal generator set to a frequency of 300MHz a power level of 0 dBm, connect the signal generator, the PC and the GB 660B data generator to the TDE (see fig 2 below).

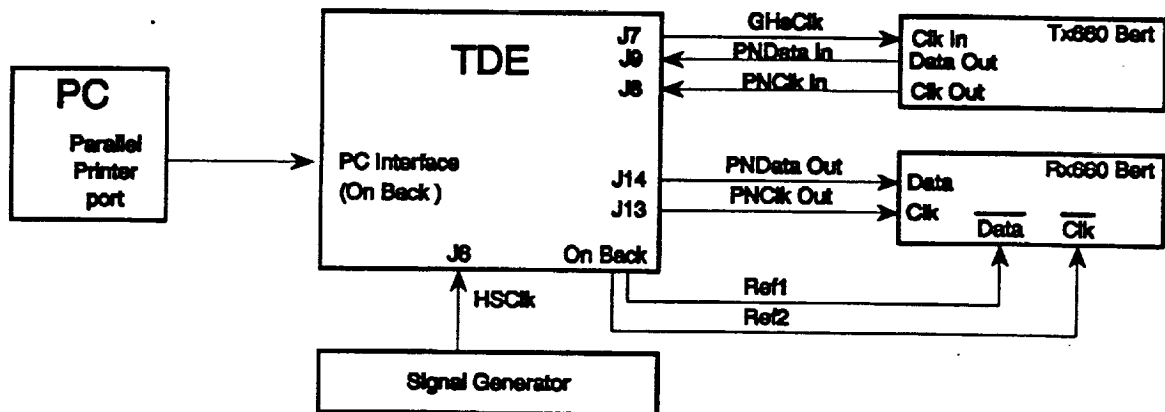


Fig 2

Insert the ATP software into the PC and run it by typing TDE. Set up the test profile #1.

NOTE: THESE TESTS WERE PERFORMED AT 250 MHz

5.3.1.1 Clocks

The following tests verify the Reference clocks out of the TDE chassis.

Set up profile #1:

FHSC Mode
 Bursted mode
 Block length = 224
 1 block per burst
 192 bit times between bursts
 16-ary
 Uncoded

Using the test box connect the leads to each of the following signals and verify the frequency :

- | | | | |
|--------------------|----------|------------|--|
| 1. TxSysClk (J15) | = 75 Mhz | <u>N/A</u> | = (bit_rate / interface_width) |
| 2. TxSysClk (J4) | = 75 Mhz | <u>OK</u> | = (bit_rate / interface_width) |
| 3. TxTQSysClk (J5) | = 75 Mhz | <u>OK</u> | = ((3*bit_rate) / (4*interface_width)) |

Set up profile #2:

FHSC Mode
Burst mode
Block length = 224
1 block per burst
192 bit times between bursts
8-ary
Uncoded

Using the test box connect the leads to each of the following signals and verify the frequency :

1. TxSysClk (J15) = 100 Mhz N/A = (bit_rate / interface_width)
2. TxSysClk (J4) = 100 Mhz OK = (bit_rate / interface_width)
3. TxTQSysClk (J5) = 75 Mhz OK = ((3*bit_rate) / (4*interface_width))

Set signal generator to 150 MHz.

Set up profile #3:

BCH Mode
Burst mode
Block length = 224
1 block per burst
192 bit times between bursts
QPSK Single-symbol
Uncoded

Connect the clock output of the data generator to the 485 O-Scope and verify the clock is gated on for 1.5 uS and off for 1.5 uS. Verify the frequency displayed by the data generator is 75 MHz (i.e. 150 MHz with a 50/50 duty cycle).

Frequency = 75 Mhz OK

Connect the TxDataClk Out on J4 to the RxDataClk In J12. Connect the PN Clock Out J13 of TDE to the Converter box and the output of the test box to the 485 O-Scope and verify the clock is on for 0.75 uSec and off for 0.75 uSec.

Clock is off for 50% of the time OK

5.3.1.2 Blockmark and Data

The following tests verify the Data and Block Mark signals of the TDE chassis for different profiles. Connect the differential inputs of the Converter box to TxData Out P2 connector and verify activity on D0 -D3 and TxBlkMk. Verify TxUnCoded and TxMode (note : TxMode signals are single ended).

D0 -D0 pins 1&9	<u>OK</u>
D1 -D1 pins 2&10	<u>OK</u>
D2 -D2 pins 3&11	<u>OK</u>
D3 -D3 pins 4&12	<u>OK</u>
TxBlkMk -TxBlkMk pins 5&13	<u>OK</u>
 TxUnCoded -TxUnCoded pins 5&13	<u>X</u>
TxMode0 pin 7	<u>OK</u>
TxMode1 pin 8	<u>OK</u>
 QPSK is mode 01	<u>OK</u>

Set signal generator to 300 MHz.

Set up profile #4:

BCH Mode
 Bursted mode
 Block length = 224
 1 block per burst
 192 bit times before the next burst.
 8-ary
 Coded

Connect the differential inputs of the Converter box to TxData Out P2 connector and verify activity on D0 -D3 and TxBlkMk. Verify TxUnCoded and TxMode (note : TxMode signals are single ended).

D0 -D0 pins 1&9	<u>xxxxxx</u>
D1 -D1 pins 2&10	<u>N/A</u>
D2 -D2 pins 3&11	<u>N/A</u>
D3 -D3 pins 4&12	<u>N/A</u>
TxBlkMk -TxBlkMk pins 5&13	<u>N/A</u>
 TxUnCoded -TxUnCoded pins 5&13	<u>N/A</u>
TxMode0 pin 7	<u>OK</u>
TxMode1 pin 8	<u>OK</u>
 8-ary is mode 10	<u>OK</u>

Set up profile #5:

BCH Mode

Bursted

2 blocks per burst

First block 224 bits second block 480 bits

0 bit times between bursts

16-ary 8-wide

Uncoded

Connect the differential inputs of the Converter box to TxData Out P2 connector and verify activity on D0 -D3 and TxBlkMk. Verify TxUnCoded and TxMode (note : TxMode signals are single ended).

D0 -D0 pins 1&9	<u>OK</u>
D1 -D1 pins 2&10	<u>OK</u>
D2 -D2 pins 3&11	<u>OK</u>
D3 -D3 pins 4&12	<u>OK</u>
TxBlkMk -TxBlkMk pins 5&13	<u>OK</u>
Verify TxBlkMk is as below	<u>OK</u>

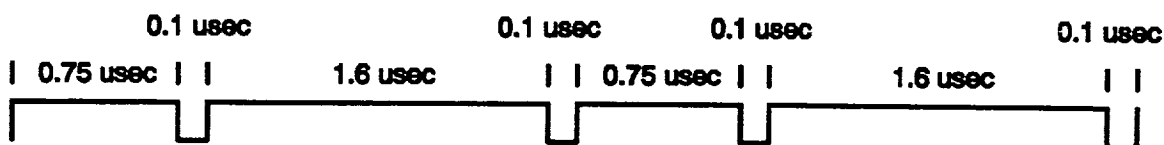


Fig 3

TxUnCoded -TxUnCoded pins 5&13	<u>X</u>
TxMode0 pin 7	<u>OK</u>
TxMode1 pin 8	<u>OK</u>
16-ary is mode 11	<u>OK</u>

Set up profile #6:

BCH Mode
Burst Mode
Block length = 224
1 block per burst
0 bits between bursts
16-ary 8-wide
Uncoded
User bits enabled

Connect the converter box to the Block Mark signal in P1 pins 5 and 13 and on the O-Scope verify the TxBlkMk signal looks as below.

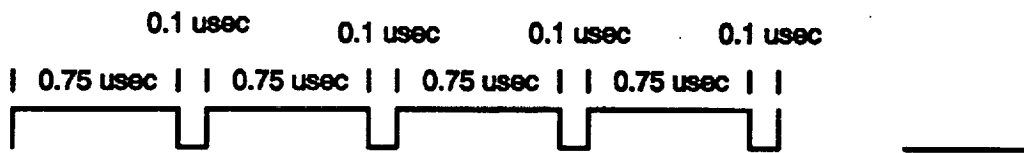


Fig 4

TxBkMkO is as shown above OK

5.3.1.3 User Bits

The following test verifies the USER bits are being generated by the TDE. Connect a O-scope probe to the USER bits out on connector P3 and verify activity (note : these are single ended signals).

USER0 - pin4, gnd on pin6	<u>OK</u>
USER1 - pin3, gnd on pin7	<u>OK</u>
USER2 - pin2, gnd on pin8	<u>OK</u>
USER3 - pin1, gnd on pin9	<u>OK</u>

5.3.2 Verify Block Profiles

The following tests verify the profiles generated by the TDE chassis

Set signal generator to 150 MHz.

Set up profile #7:

- FHSC Mode
- Bursted mode
- 2 blocks per burst
- 48 bit times between bursts
- length of first block 224 bits
- length of second block 480 bits
- QPSK
- Coded

Connect the converter box to the Block Mark signal in P1 pins 5 and 13 and on the O-Scope verify the TxBlkMk signal looks as below (clocks refer to TxSysClkO).

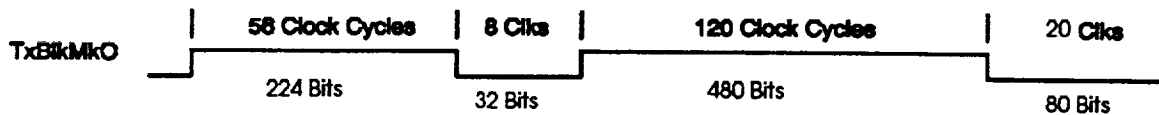


Fig 5

TxBkMkO is as shown above OK

Set up profile #8:

- FHSC Mode
- Bursted mode
- 2 blocks per burst
- 48 bit times between bursts
- length of first block 480 bits
- length of second block 224 bits
- QPSK
- Coded

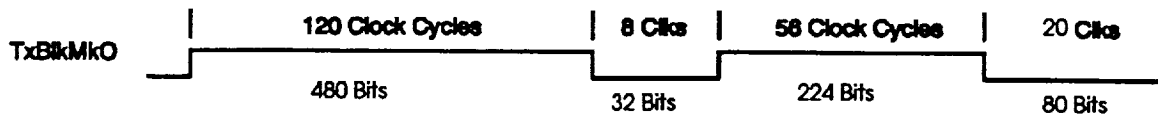


Fig6

TxBkMkO is as shown above OK

5.4 Functional Testing

Connect the RxBert signals to the uWave Logic error detector PNClk Out, J13, to Clock In and PNData Out, J14, to Data In. In addition connect the Ref1 out to the -Clock In of the error detector and the Ref2 Out to the -Data In of the error detector. Ref1 and Ref2 are on the back panel of the TDE chassis.

5.4.1 Noise Generator, QPSK

The following functional tests validate the noise generator circuits performance for QPSK signals.

Set up profile #9:

- BCH Mode
- Burst Mode
- 1 block per burst
- Block length = 256
- 0 bit times between bursts
- QPSK Single-symbol
- Uncoded
- $E_b/N_o = 8$ dB

Measure the Bit error rate $1.0 \times 10^{-4} < \underline{2.0E-4} < 3.0 \times 10^{-4}$

Set up profile #10:

- BCH Mode
- Burst Mode
- 1 block per burst
- Block length = 256
- 0 bit times between bursts
- QPSK Single-symbol
- UnCoded
- $E_b/N_o = 10$ dB

Measure the Bit error rate $3.0 \times 10^{-6} < \underline{4.5E-6} < 6.0 \times 10^{-6}$

Set up profile #11:

- BCH Mode
- Burst Mode
- 1 block per burst
- Block length = 256
- 0 bit times between bursts
- QPSK Single-symbol
- Uncoded
- $E_b/N_o = 12$ dB

Measure the Bit error rate $7.0 \times 10^{-9} < \underline{1.6E-8} < 2.0 \times 10^{-8}$

5.4.2 Noise Generator, 16-ary

The following functional tests validate the noise generator circuits performance for 16-ary signals.

Profile #12:

BCH Mode
Continuous Mode
16-ary 8-wide
Uncoded
Eb/No = 16 dB

Measure the Bit error rate $1.0 \times 10^{-4} < \underline{1.5E-4} < 2.0 \times 10^{-4}$

Profile #13:

BCH Mode
Continuous Mode
16-ary 8-wide
Uncoded
Eb/No = 18 dB

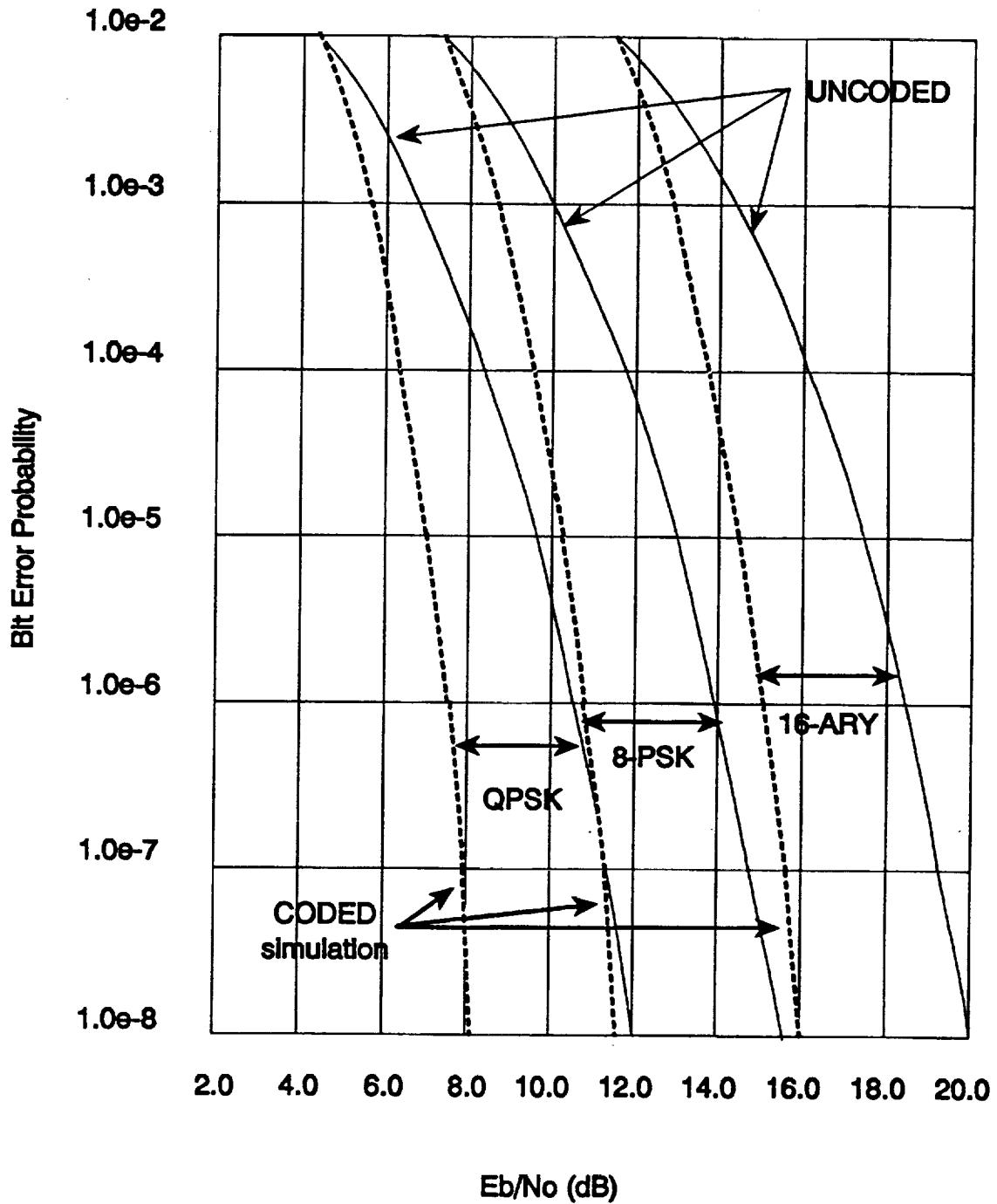
Measure the Bit error rate $2.0 \times 10^{-6} < \underline{4.6E-6} < 6.0 \times 10^{-6}$

Profile #14:

BCH Mode
Continuous Mode
16-ary 8-wide
UnCoded
Eb/No = 20 dB

Measure the Bit error rate $7.0 \times 10^{-9} < \underline{2.3E-8} < 4.0 \times 10^{-8}$

6.0 Theoretical Performance curves




Testing Performed By :
 QC Witness/ Monitor :
 Accepted By :

Greg P. Segallis, Harris 6/16/92
Robert Jones, NASA LeRC


APPENDIX B

FHSC BCH ASIC Acceptance Test Procedure


For NASA Lewis Research Center
Contract NAS3-25087

 7/27/92

Greg P Segall Date
Lead Engineer

 7/28/92

Jim V Wernlund Date
Staff Engineer

 7-27-92

Glen Corry Date
Program Manager

Robert Jones Date
NASA LeRC



HARRIS

Harris Government Communication Systems Division

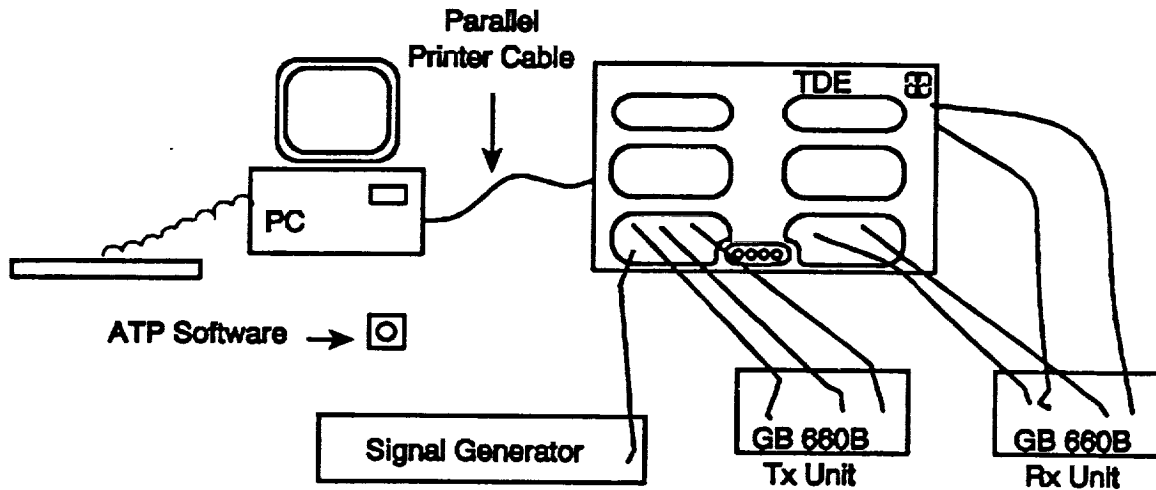
ESD 22580

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NOTE: ACTUAL TEST RESULTS ARE UNDERLINED ITALICS

1.0 Scope

This document describes the tests necessary to verify proper operation of the BCH ASIC. AC tests verify the ASIC timing specifications. Performance tests verify the functionality of the various modes of operation as well as the coding gain performance.



2.0 Applicable Documents

ESD 22581 BCH Specification
Assy- 179697 TDE Chassis Assembly
Assy- 179704 BCH Card Assembly
ATP Software

3.0 Required Test Equipment

Model	Description	S/N	Cal Due
WaveTek 3510	Signal Generator	150154	9/92
O-Scope	Tektronix 485	150873	9/92
Hp 5334A	Counter/ DVM		
1630G	Hp Logic Analyzer	150389	10/92
Tx660B	uWave Logic Data Generator	134450	
Rx660B	uWave Logic Error Detector	134451	
T-TBD	Converter box (#TBD)	001	
Assy 179697	TDE Chassis		
A6302	Tektronix current probe		

4.0 Specifications

4.1 Power Supplies

The tests shall be performed with the TDE power supplies adjusted to within 5% of their nominal value.

4.2 Environment

The tests shall be performed at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$

5.0 Test Procedure

5.1 Purpose

The purpose of the following tests is to verify proper electrical characteristics, functional performance and operational performance of the BCH ASIC. This will validate the fabrication process, logic design, and conceptual design

5.2 AC Testing

Turn on the TDE and verify the front panel voltage indicator lights function.

+5.0 Volts	<u> +5.05 </u>
-2.0 Volts	<u> -2.06 </u>
-4.5 Volts	<u> -4.56 </u>
-5.2 Volts	<u> -5.21 </u>

Turn off the TDE.

With the Signal generator set to a frequency of 10 MHz and a power level of 3 dBm, connect the signal generator, the PC and the GB 660B data generator to the TDE (see fig 3 below).

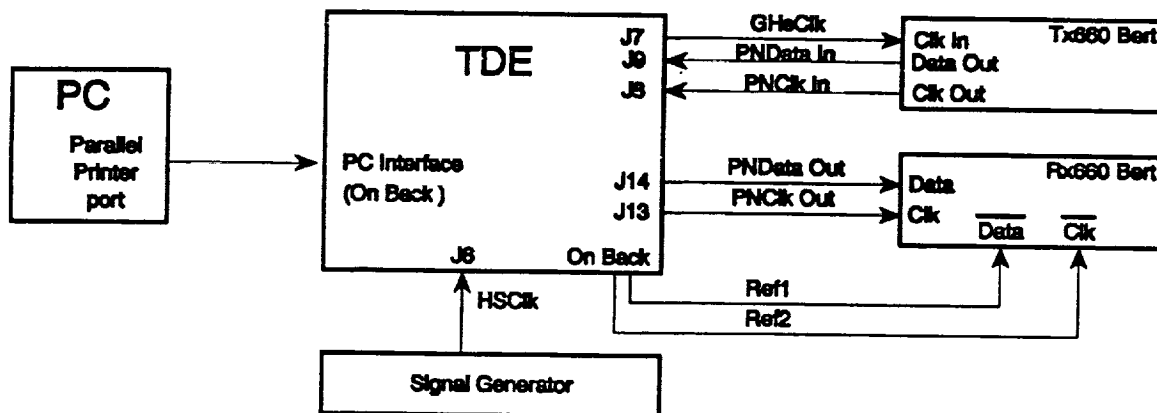


Fig 3

Insert the ATP software into the PC and run it by typing TDE.

5.2.1 Control & Data Timing

The purpose of these tests is to verify the proper timing relationships for the Clocks, Data and Block Mark signals

Set up test profile #1:

BCH Mode
16-PSK 8-wide
Continuous mode
Uncoded

Put a scope probe on pin K3 and N1 of the BCH ASIC and verify the timing of the clocks TxDatClkE and TxDatClkL as shown below.

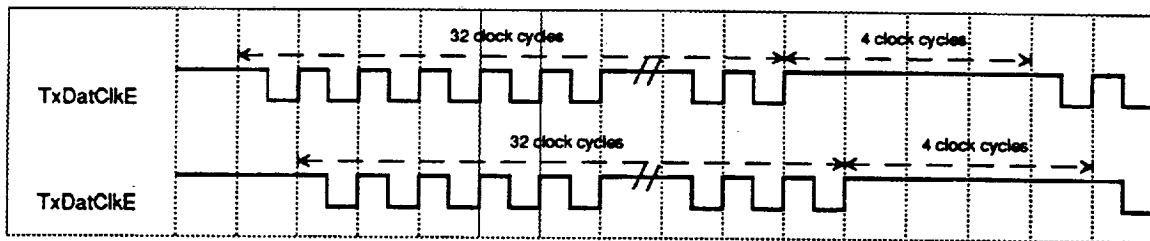


Fig 4

TxDatClkE is as shown above OK

TxDatClkL is as shown above OK

Put a scope probe on pin P4 of the BCH ASIC and verify the signal TxBlkMkO is as shown below.

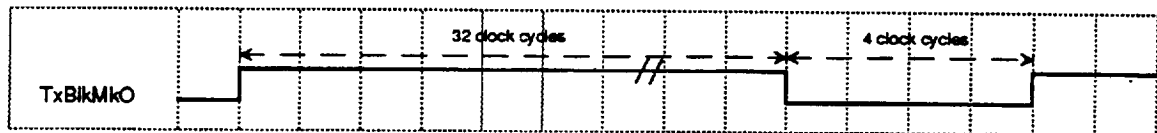


Fig 5

TxBlkMkO is as shown above OK

Put a scope probe on pin N4 of the BCH ASIC and verify the signal TxCodeClkO is present.

A continuous clock exists at TxCodeClk OK

Set up Profile #2:

BCH Mode

16-PSK 8-wide

Burst mode

1 block per burst

Block length = 256 bits

0 bit times between bursts

UnCoded

Put a scope probe on pin M5 and N1 of the BCH ASIC and verify the timing relationship between TxBlkMkI and TxDatClkE as shown below.

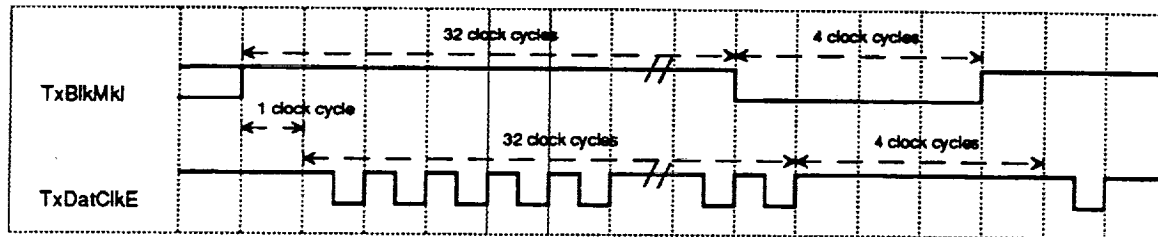


Fig 6

Timing is as shown above OK

Put a scope probe on pin M5 and K3 of the BCH ASIC and verify the timing relationship between TxBlkMkI and TxDatClkL as shown below, .

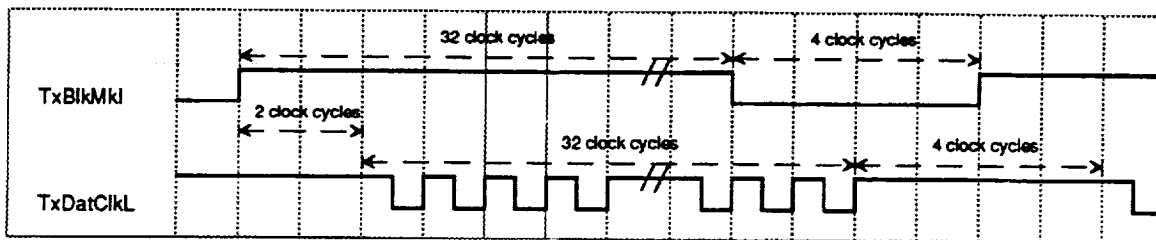


Fig 7

Timing is as shown above OK

Set up profile #3:

BCH Mode

Burst mode

1 block per burst

Block length = 224

1280 bit times between bursts

QPSK Single-Symbol

Coded

Parity Disabled

Put a scope probe on pins P4 and H3 and verify the timing relationship between TxBlkMkO and TxGatClk as shown below.

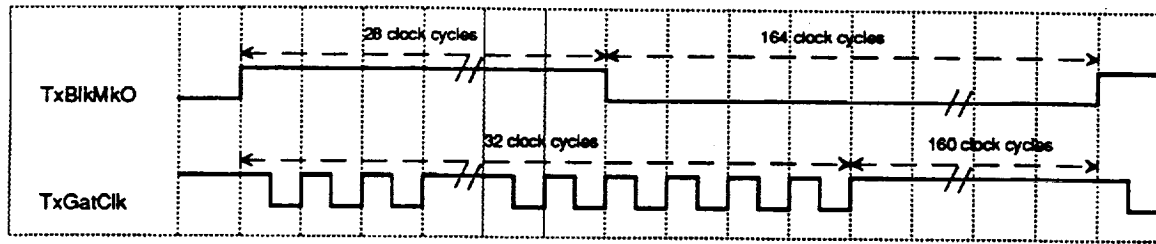


Fig 8

Timing is as shown above OK

Put a scope probe on pins D12 and G13 and verify the timing relationship between RxBlkMkO and RxDatClk as shown below.

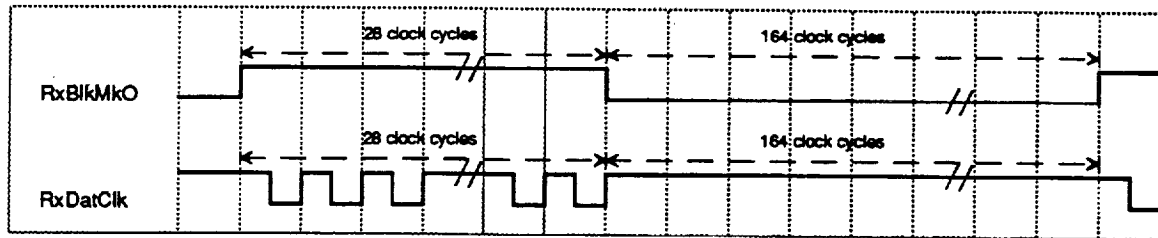


Fig 9

Timing is as shown above OK

5.2.2 Parity Bit Timing

The purpose of this test is to verify the parity bits are clocked out of the BCH ASIC chip when parity is enabled.

Set up profile #4 :

- BCH Mode
- Burst mode
- 1 block per burst
- Block length = 256
- 1280 bit times between bursts
- QPSK Single-Symbol
- Coded
- Parity enabled

Put a scope probe on pins G13 and D12 and verify the timing relationship between RxDataClk and RxBlkMkO shown below.

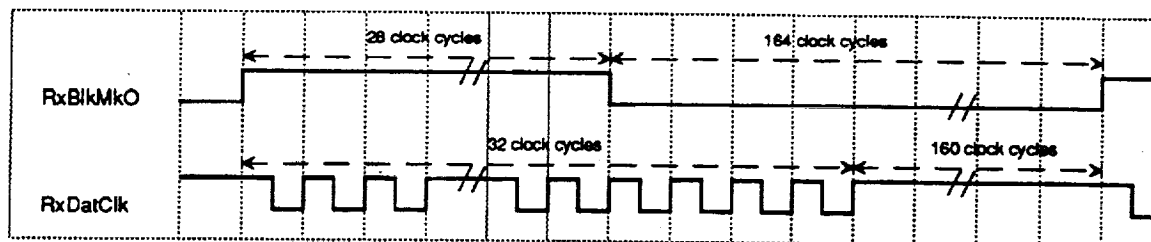


Fig 10

Timing is as shown above OK

5.3 Performance Testing

5.3.1 Continuous Mode BER Performance

Profiles #5 - 11 are intended to demonstrate the performance gains obtained by the BCH CODEC ASIC in the continuous mode for both QPSK and 16-ary modulation modes. In addition, they demonstrate the CODEC's ability to acquire the code word position.

Set up profile #5:

BCH Mode
Continuous Mode
QPSK Single Symbol
Coded
Eb/No = 99

Verify error free performance

X Problem with DATCLKE - refer to Final Report. BCH is LOCKED.

Profile #6:

BCH Mode
Continuous Mode
QPSK Single Symbol
Coded
Eb/No = 6 dB

Measure the Bit error rate X < 4.0×10^{-4}

Profile #7:

BCH Mode
Continuous Mode
QPSK Single Symbol
Coded
Eb/No = 7 dB

Measure the Bit error rate X < 1.0×10^{-5}

Profile #8:

BCH Mode
Continuous Mode
QPSK Single Symbol
Coded
Eb/No = 8 dB

Measure the Bit error rate X < 7.0×10^{-8}

Profile #9:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 14 dB

Measure the Bit error rate 2.2E-5, 4.5E-5 < 7.0×10^{-5}

Profile #10:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 15 dB

Measure the Bit error rate 3.8E-7, 4.1E-7 < 2.0×10^{-6}

Profile #11:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 16 dB

Measure the Bit error rate 1E-9, 3.5E-9 < 2.0×10^{-8}

5.3.2 Continuous Mode Codeword Acquisition Time

Profiles #12 - 19 are used to measure codeword position acquisition times for the CODEC's 8 different lock thresholds.

Set signal generator to 8 KHz. Acquisition is indicated by the LED CR2 mounted on the BCH card.

Profile #12:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 16 dB
Lock Threshold 0

Measure the time to acquisition 5.12.13 seconds

Profile #13:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 16 dB
Lock Threshold 1

Measure the time to acquisition 11.13.16 seconds

Profile #14:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 16 dB
Lock Threshold 2

Measure the time to acquisition 17.16.14 seconds

Profile #15:

BCH Mode
Continuous Mode
16-ary 8-wide
Coded
Eb/No = 16 dB
Lock Threshold 3

Profile #25:

BCH Mode
Burst Mode
QPSK Single-symbol
Coded
10 Blocks of length 224
1 Block of length 480
32 Bit times between bursts
Eb/No = 8 dB

Measure the Bit error rate 1.0E-8 < 1.0×10^{-7}

Profile #26:

BCH Mode
Burst Mode
16-ary Single-symbol
Coded
10 Blocks of length 224
1 Block of length 480
32 Bit times between bursts
Eb/No = 14 dB

Measure the Bit error rate 3.0E-5 < 2.0×10^{-4}

Profile #27:

BCH Mode
Burst Mode
16-ary Single-symbol
Coded
10 Blocks of length 224
1 Block of length 480
32 Bit times between bursts
Eb/No = 15 dB

Measure the Bit error rate 7.0E-7 < 3.0×10^{-6}

Put the signal USER error out of the back panel on the counter and verify no activity OK

Profile #31:

BCH Mode
Burst Mode
16-ary 8-wide
Coded
10 Blocks of length 256
1 Block of length 512
32 Bit times between bursts
Eb/No = 14 dB
User bits enabled

Put the signal USER error out of the back panel on the counter and verify activity OK

5.3.7 Throughput Delay

Profiles #32 and 33 are used to establish the total delay through the encoder and decoder and show it is independent of the mode Coded/UnCoded.

Profile #32:

BCH Mode
Burst mode
1 block per burst
Block length = 256
1280 bit times before the next burst.
16-ary 8-wide
Coded

Put a O-scope probe on TxBlkMkI pin M5 and a O-scope probe on RxBlkMkO pin D12 and measure the delay between the two signals.

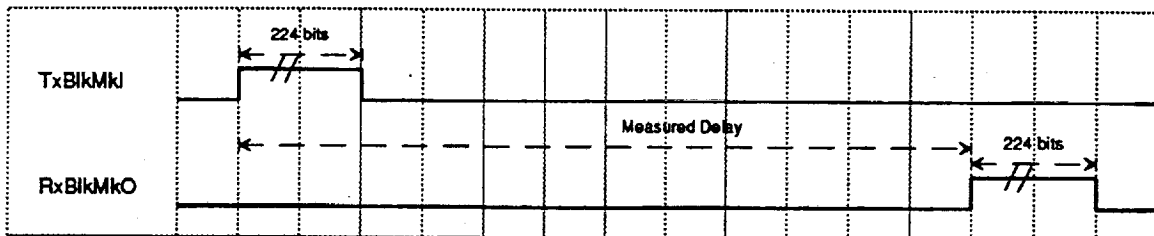


Fig 11

Measured Delay is 986 BITS (16-ary 8-wide)
948 BITS (16-ary Single-symbol)
920 BITS (QPSK Single-symbol)

Profile #33 :

BCH Mode
Burst mode
1 block per burst
Block length = 256
1280 bit times before the next burst.
16-ary 8-wide
Uncoded

Put a O-scope probe on TxBlkMkI pin M5 and a O-scope probe on RxBlkMkO pin D12 and measure the delay between the two signals. Compare the two delays measured above, they should be the same.

Measured Delay is 986 BITS (16-ary 8-wide)
The delays are the same OK

5.3.8 Single-Symbol Interface

Profiles #34 and 35 are used to demonstrate the single-symbol interface capability of the BCH ASIC.

Profile #34 :

BCH Mode
Burst mode
1 block per burst
Block length = 224
1280 bit times before the next burst.
QPSK Single-symbol
Coded
Eb/No = 99

Put a scope probe on pins D12 and G13 and verify the timing relationship between RxBlkMkO and RxDatClk shown below.

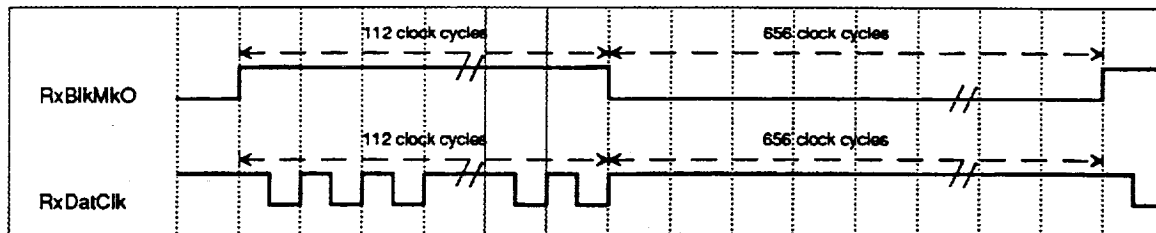


Fig 12

Timing is as shown above OK
Performance is error free OK

Profile #35:

BCH Mode
Burst mode
1 block per burst
Block length = 256
1280 bit times before the next burst.
16-ary Single-symbol
Coded
Eb/No = 99

Put a scope probe on pins D12 and G13 and verify the timing relationship between RxBlkMkO and RxDatClk shown below.

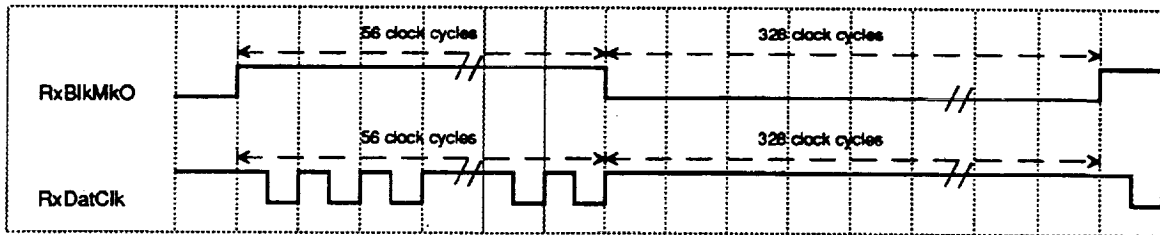


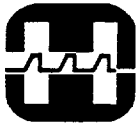
Fig 13

Timing is as shown OK
Performance is error free OK

Testing Performed By : Greg P Segallis, Harris 6/15/92
QC Witness/ Monitor : Robert Jones, NASA LeRC
Accepted By : _____

Appendix C

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BCH ASIC
PN 66948 179696

PRELIMINARY

Features

- Encoder and Decoder on a single chip
- Up to 4 dB of gain at 10^{-8} BER
- CMOS design
- Modem Ambiguity Resolution

Circuitry

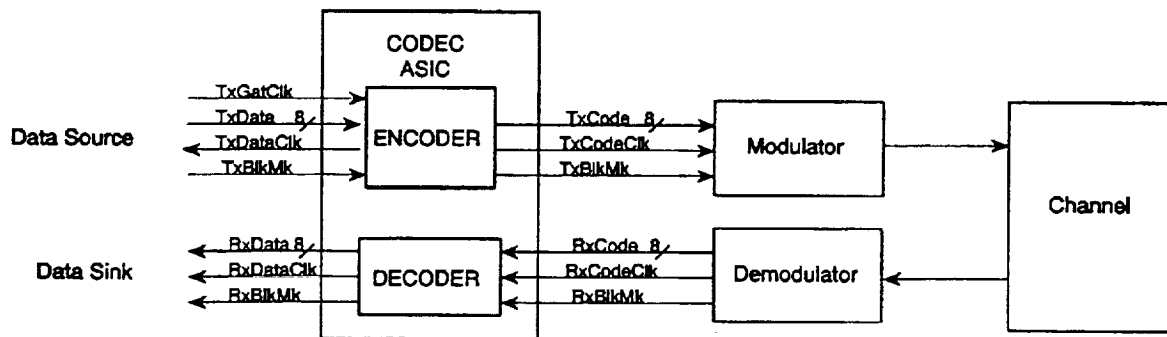
- Bursted or Continuous formats
- Code Rates of 7/8 to 15/16
- Interface widths of 1, 2, 4 or 8 bits
- Programmable lock and unlock thresholds
- Outputs error locations for soft decision applications
- Available in 132 Lead Pin Grid Array(PGA)

Description

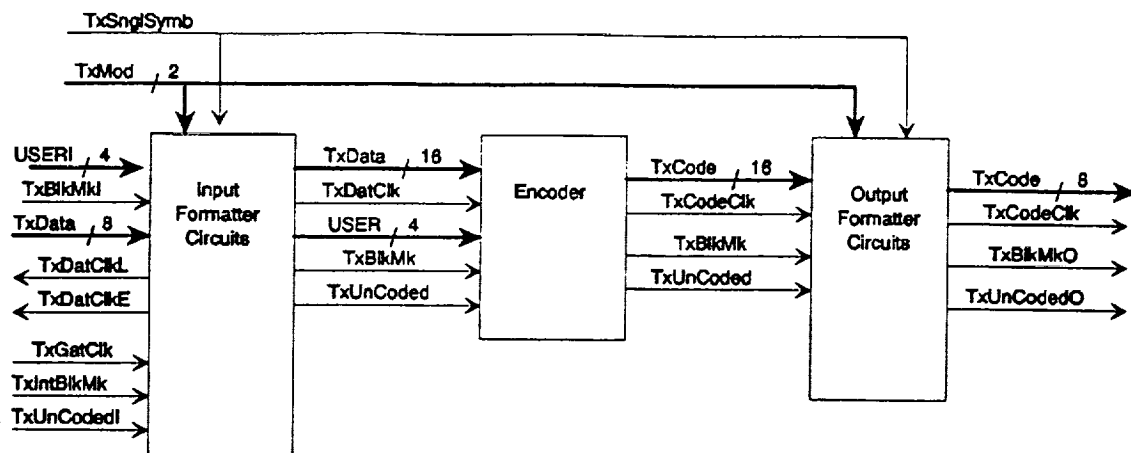
The Harris -NASA CODEC is a high speed, low power CMOS triple error correcting Bose-Chaudhuri-Hocquenghem (BCH) block CODEC. Data can be clocked into the device 1,2, 4 or 8 bits at a time.

A single control line (block Mark) is used to control the length of the block and to concatenate blocks. When the CODEC is used in the continuous mode the CODEC can generate the block mark signal internally. In either case the CODEC generates a gated clock for clocking data to and from the user. Several mode control signals are sampled on the rising edge of the block mark signal. From block to block these mode signals are allowed to change resulting in the CODEC being able to change modes on block boundaries. Programmable lock and unlock thresholds enable the CODEC to operate reliably under a variety of modulation modes and environments.

Many of the control signals internal to the CODEC along with the Error locations corrected by the CODEC are also available. These signals enable the CODEC to be used in more elaborate coding schemes such as Chase soft decision decoding.

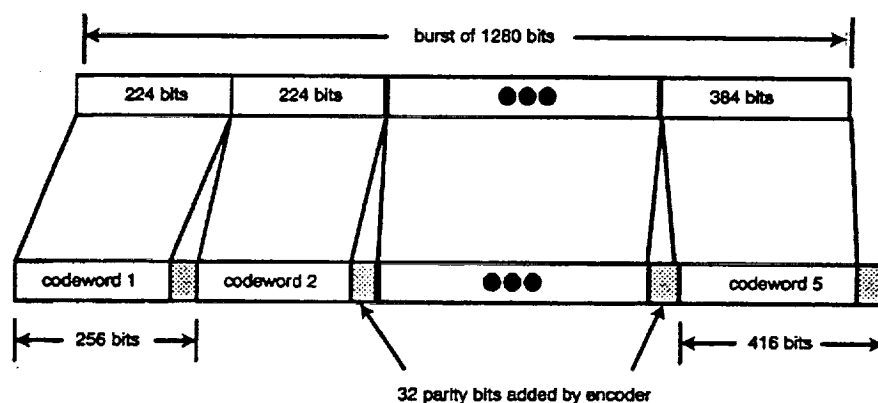


Typical Application



Encoder Block Diagram

The encoder circuits consist of the Input Formatter, the Encoder, and the Output Formatter. The input formatter generates the gated clocks TxDatClkL and TxDatClkE for clocking data from the user and formats the input data from the user interface width (1, 2, 4 or 8 bits) to the 16 bit word processed by the encoder. In addition the Input Formatter registers the 4 USERI bits inserted by the encoder into the code word. These 4 bits are unprotected bits inserted at the end of a code word. They are provided for order wire applications. The code word is formatted back into the user interface width by the Output Formatter. The signals TxBlkMkO and TxUnCodedO are the signals TxBlkMkI and TxUnCodedI delayed by the encoder delay. They are coincident with code word boundaries. Bursts of almost any length can be generated by concatenating blocks. If the encoder is used in the continuous mode it can generate its own code word boundaries. If the control line TxIntBlkMk is forced high a Block Mark signal is internally generated. This results in code words of length 288 bits. Below is an example of a burst of length 1280 bits formed by the concatenating of 4 code words of length 256 bits and one code word length 416 bits.

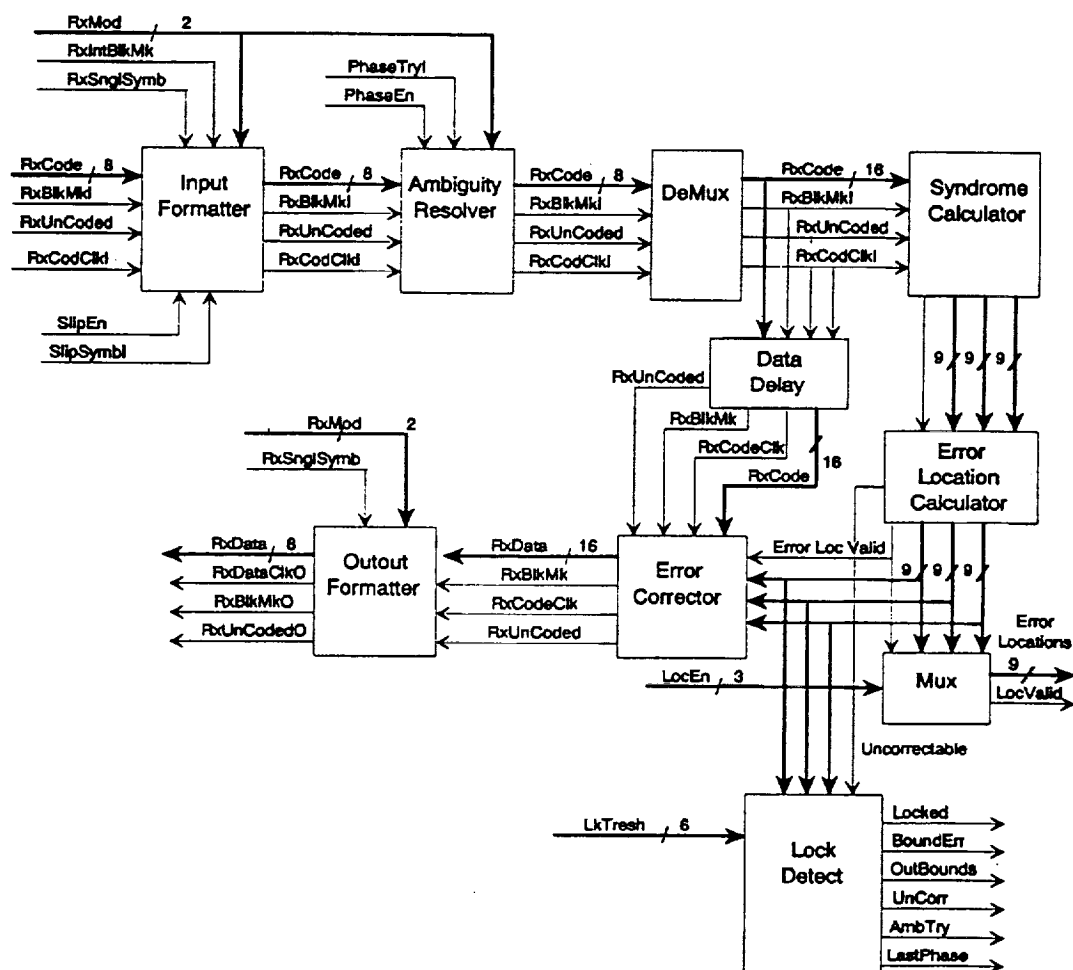


Concatenated blocks

Encoder definitions:

- USERI[3-0] : Four input lines for the unprotected USER bits to the encoder. These bits are sampled by the Block Mark signal.
- TxGatClk : Continuous clock to the encoder. This clock is "anded" with the Block Mark signal to generate the gated clocks to the user. The rate of this clock is the encoded symbol rate.
- TxDat[7-0] : The user data interface. Legal interface widths are 1, 2, 4 and 8.

- TxBlkMkI :** The user supplied Block Mark signal. Legal signal is 224 bits to 480 bits high ,in 16 bit increments, followed by at least 32 bits low. Note if block mark is left low for more than 32 bit times it must remain low for at least 40 bit times This is because the burst mode of operation is assumed and resets occur at the end of a burst. For an the interface width of 8 bits a valid signal is 28 to 60 TxGatClks high, in 2 clock increments, followed by at least 4 TxGatClks low.
- TxUnCodedI :** A logic 1 indicates the block is not to be coded. This signal is sampled on the rising edge of TxBlkMkI.:Note this does not effect the delay of the encoder.
- TxMode[0-1] :** These signals along with TxSinglSymb are used to specify the interface width.
- TxSinglSymb :** A logic 1 indicates the interface width is other than 8 bits.
- TxIntBlkMk :** A logic 1 causes the encoder to generate the block mark signal internally. The internal block length is 288 bits.
- TxDatClkE :** One of two gated clocks generated by the encoder. The clock turns on one clock cycle after TxBlkMkI goes high. This is one clock cycle before the encoder expects to see data.
- TxDatClkL :** One of two gated clocks generated by the encoder. This clock turns on two clock cycles after TxBlkMkI goes high.
- TxCode[7-0] :** The user code interface width. Legal interface widths are 1, 2, 4 and 8. This interface is always the same as the TxDat[7:0] interface.
- TxCodeClk :** A gated clock generated by the encoder for clocking data to the modulator. It is active for the duration of a burst. In the continuous mode it is a continuous clock.
- TxBlkMkO :** The TxBlkMkI signal delayed by the delay of the encoder.
- TxUnCodedO :** The TxUnCodedI signal delayed by the delay of the encoder.
- TxReset :** A logic 1 resets all the registers with in the encoder.



Decoder Block Diagram

The decoder circuits consist of the following functional blocks the Input Formatter, the Ambiguity Resolver, the Syndrome Calculator, the Error Location Calculator, the Data Delay, the Output Formatter and the Lock Detector. The actual decoding function is performed by the Syndrome Calculator, the Error Location Calculator and the Error Corrector circuits. The Input Formatter formats the user interface to the 8 bit interface of the Ambiguity Resolver while the Output Formatter formats the 16 bit interface of the encoder to the user interface.

Code words are clocked into the decoder with the RxCodClkI. When the chip is used in the burst mode the control signal RxBlkMkI is used to indicate code word boundaries. If RxIntBlkMk is high the Input Formatter circuits assume the decoder is in the continuous mode and a Block Mark is internally generated. In this mode SlipSymbEn to the Input formatter is forced high and AmbTry from the Lock Detector is strapped to SlipSymbI. The Input formatter then slips the internally generated Block Mark signal until it is coincident with the incoming code word boundaries.

The Ambiguity Resolver is user to resolve PSK carrier phase ambiguities. This circuit is able to resolve BPSK, QPSK and 16 PSK phase ambiguities. This circuit is enabled by a logic 1 on the PhaseEn pin to the Ambiguity resolver. In the continuous mode if AmbTry is tied to PhaseTryI and LastPhase is tied to SlipSymbI the Input Formatter, in conjunction with the Ambiguity Resolver and the Lock Detector, can resolve both the code word boundaries and carrier phase ambiguities.

The Data Delay circuits are pipe lined registers used to delay the code word while the Syndrome Calculator and the Error Location Calculator perform their functions. The delay (in bits) of the decoder is independent of the mode of operation.

The Lock Detector generates several signals which can be used to evaluate the condition of the encoder. The signal Locked indicates the decoder is locked. Six control lines select between 8 set thresholds and 8 release thresholds. In addition to the Locked signal the decoder outputs BoundErr OutBounds and UnCorr. These signals indicate if the errors occurred at the code word boundaries, if the errors occurred outside the code word boundaries (this is only valid for code words less than (480, 512) bits) or uncorrectable errors occurred within a single code word.

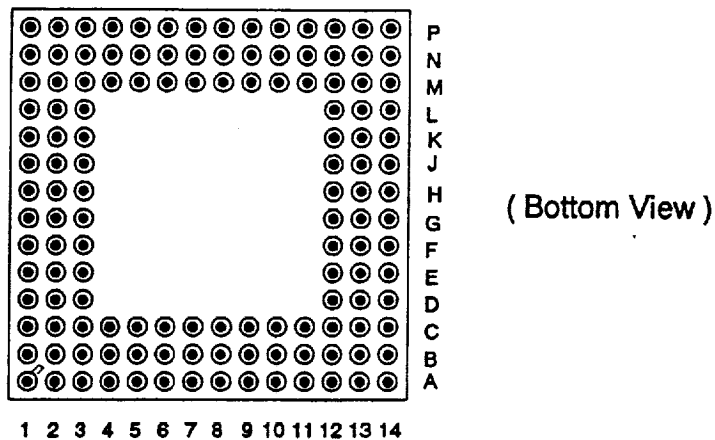
The encoder also outputs the bit locations within a code word the encoder changed. This information is available for applications where multiple decoders are used to improve coding performance. One such application is the Chase Soft decision decoding scheme which is currently under development at Harris. These bits could also be used to monitor the bit error rate performance of the link.

Decoder Definitions:

- RxCode[7-0] : The decoder code word interface. Legal interface widths are 1, 2, 4 and 8 bits.
- RxBlkMkI : The user supplied encoder block mark signal. This signal is used to indicate valid code word boundaries to the decoder.
- RxCodClk : The user supplied decoder clock. This is a continuous clock at the coded interface rate.
- RxUnCodedI : A logic 1 indicates the next block is uncoded. This signal is sampled on the rising edge of RxBlkMkI. Note it does not effect the delay of the decoder.
- RxSinglSymb : A logic one sets the interface width to the symbol width indicated by the signals RxMod[1-0]. Note 8-ary (3 bit interface) is not a legal interface width.
- RxMod[1-0] : Indicates the signaling mode, BPSK, QPSK, 8-PSK or 16-PSK. This information is used by the interface mode control circuits and the carrier phase ambiguity circuits. Note the ambiguity circuits cannot resolve 8-PSK carrier phase.
- RxIntBlkMk : A logic 1 causes the decoder to generate the block mark signal internally. In this mode the blocks are forced to 288 bits.
- LocEn[2-0] : Three lines used to select between 8 lock thresholds.
- LocEn[5-3] : Three lines used to select between 8 unlock thresholds.
- RxDat[7-0] : Interface used to transfer decoded data to the user. Legal interface widths are 1, 2, 4 and 8 bits.
- RxDatClk : A gated clock used to transfer decoded data back to the user.
- RxBlkMkO : The RxBlkMkI signal delayed by the delay of the decoder.
- RxUnCodedO : The RxUnCodedI signal delayed by the delay of the decoder.
- UserO[0-3] : The 4 USER bits removed by the decoder These are the 4 USER bits appended by the encoder
- Locked : A logic 1 indicates the decoder is locked.

BoundErr : A logic 1 indicates the errors detected or corrected are concentrated at the code word boundaries.
OutBounds : A logic 1 indicates the errors detected were outside of the code word boundaries. This signal only has meaning for code words smaller than 512 bits.
UnCorr : A logic 1 indicates there were more than 3 errors in a code word.
AmTry : A logic 1 indicates there is a problem with either the carrier phase or RxBlkMkI phase.
Last Phase : A logic one indicates the carrier phase ambiguity circuits have tried all the possible phases for the modulation mode indicated.
ErrLoc[8-0] : Interface used to transfer the error locations corrected in by the decoder. Note location 0 indicates no bit change occurred.
LocValid : A logic 1 indicates the error locations calculated by the decoder are valid.
LocEn1 : A logic 1 forces the first error location corrected to appear on the ErrLoc interface.
LocEn2 : A logic 1 forces the second error location corrected to appear on the ErrLoc interface.
LocEn3 : A logic 1 forces the third error location corrected to appear on the ErrLoc interface.
ParityEn : A logic 1 allows the decoded code word parity bits to be clocked out at the end of the data bits.
PhaseEn : A logic 1 enables the carrier phase ambiguity circuits.
PhaseTryI : A rising edge causes the phase ambiguity circuits to try the next carrier phase.
SlipEn : A logic one enables the internal block mark generator slip symbol circuits.
SlipSymbl : A rising edge causes the internal block mark generator circuits to slip one RxCodClk cycle.
Fault : A logic one indicates the decoder fault isolation circuits have detected a fault. The CODEC chip has failed.
RxReset : A logic 1 resets all the registers in the decoder.
TxScan : A logic 1 forces the encoder into the scan test mode.
TxScanClk : Encoder scan clock.
TxScanIn : Encoder scan testing input.
TxScanO : Encoder scan testing output.
RxScan : A logic 1 forces the decoder into the scan test mode.
RxScanClk : Decoder scan clock.
RxScanIn : Decoder scan testing input.
RxScanO : Decoder scan testing output.

132 - Pin Ceramic Pin Grid Array



USERI3	B1	SLIPEN	M10	BOUNDERR	A2
USERI2	C2	SLIPSYMBI	N11	OUTBOUNDS	B12
USERI1	D3	PHASEEN	C12	LASTPHASE	B7
USERI0	C1	PHASETRYI	B13	UNCORR	M7
TXGATCLK	H3	LOCEN3	B11	AMBTRY	B3
TXDAT7	H2	LOCEN2	A11	USERO3	M6
TXDAT6	H1	LOCEN1	C10	USERO2	N6
TXDAT5	J1	LKTHRS5	C9	USERO1	P6
TXDAT4	J2	LKTHRS4	B9	USERO0	P7
TXDAT3	L1	LKTHRS3	A9	RXDAT7	K13
TXDAT2	K2	LKTHRS2	A8	RXDAT6	K14
TXDAT1	M1	LKTHRS1	B8	RXDAT5	J12
TXDAT0	L2	LTTHRS0	C8	RXDAT4	J13
TXBLKMKI	M5	RXCOD7	F13	RXDAT3	J14
TXUNCODEDI	D1	RXCOD6	F12	RXDAT2	H14
TXMOD1	F1	RXCOD5	E14	RXDAT1	H13
TXMOD0	G1	RXCOD4	D14	RXDAT0	H12
TXSNGLSYMB	E3	RXCOD3	E13	RXDATCLK	G13
TXINTBLKMK	G3	RXCOD2	C14	RXBLKMKO	D12
TXDATCLKL	K3	RXCOD1	D13	RXUNCODEDO	P14
TXDATCLKE	N1	RXCOD0	E12	RXRESET	N5
TXCODE7	L3	RXCODCLKI	B14	RXSCAN	M14
TXCODE6	P1	RXBLKMKI	A14	RXSCANCLK	L12
TXCODE5	N2	RXUNCODEDI	N13	RXSCANIN	M13
TXCODE4	M3	RXMOD1	L13	RXSCANOUT	N14
TXCODE3	P2	RXMOD0	L14	TEST/NORM	P12
TXCODE2	N3	RXSNGLSYMB	M12	VCC	A1, A10, B2, C7, C13, G12, G14, J3, M11
TXCODE1	M4	RXINTBLKMK	K12	GND	B10, C4, F14, G2, K1, M2, N7, N12, P5, P13,
TXCODE0	P3	LOCVALID	A12	TEST8-0	M8, N8, P8, P9, N9, M9, P10, P11, N10
TXCODECLK	N4	ERRLOC8	A6		
TXBLKMKO	P4	ERRLOC7	B6		
TXUNCODEDO	D2	ERRLOC6	C6		
TXRESET	C3	ERRLOC5	A5		
TXSCAN	F2	ERRLOC4	A4		
TXSCANCLK	F3	ERRLOC3	B5		
TXSCANIN	E1	ERRLOC2	A3		
TXSCANOUT	E2	ERRLOC1	B4		
FAULT	A7	ERRLOC0	C5		
PARITYEN	A13	LOCKED	C11		

Transmit Mode Select

TxMode1	TxMode0	
0	0	BPSK
0	1	QPSK
1	0	8-ARY
1	1	16-ARY

Receive Mode Select

RxMode1	RxMode0	
0	0	BPSK
0	1	QPSK
1	0	8-ARY
1	1	16-ARY

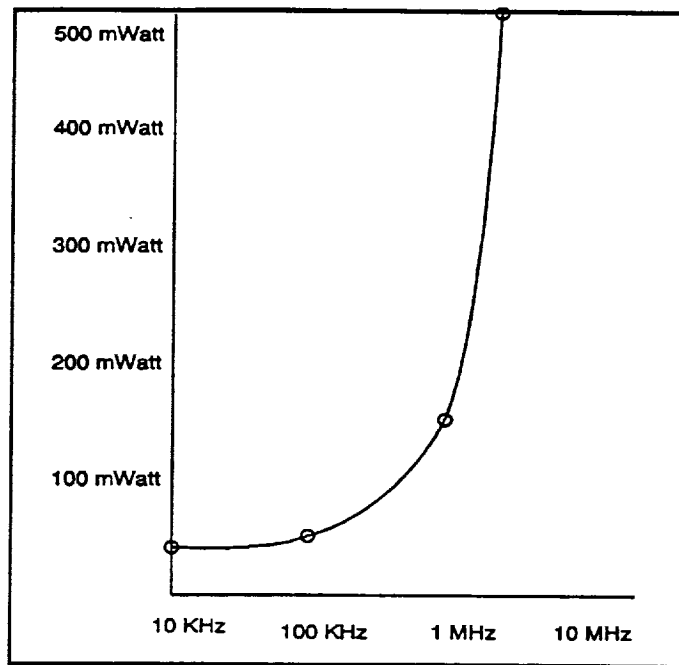
Lock Tresholds

LkTresh2	LkTresh1	LkTresh0	
0	0	0	2 of 8 uncorrectable blocks
0	0	1	3 of 8 uncorrectable blocks
0	1	0	4 of 8 uncorrectable blocks
0	1	1	6 of 8 uncorrectable blocks
1	0	0	4 of 16 uncorrectable blocks
1	0	1	6 of 16 uncorrectable blocks
1	1	0	8 of 16 uncorrectable blocks
1	1	1	12 of 16 uncorrectable blocks

UnLock Tresholds

LkTresh5	LkTresh4	LkTresh3	
0	0	0	15 of 32 uncorrectable blocks
0	0	1	17 of 32 uncorrectable blocks
0	1	0	19 of 32 uncorrectable blocks
0	1	1	23 of 32 uncorrectable blocks
1	0	0	30 of 64 uncorrectable blocks
1	0	1	34 of 64 uncorrectable blocks
1	1	0	38 of 64 uncorrectable blocks
1	1	1	46 of 64 uncorrectable blocks

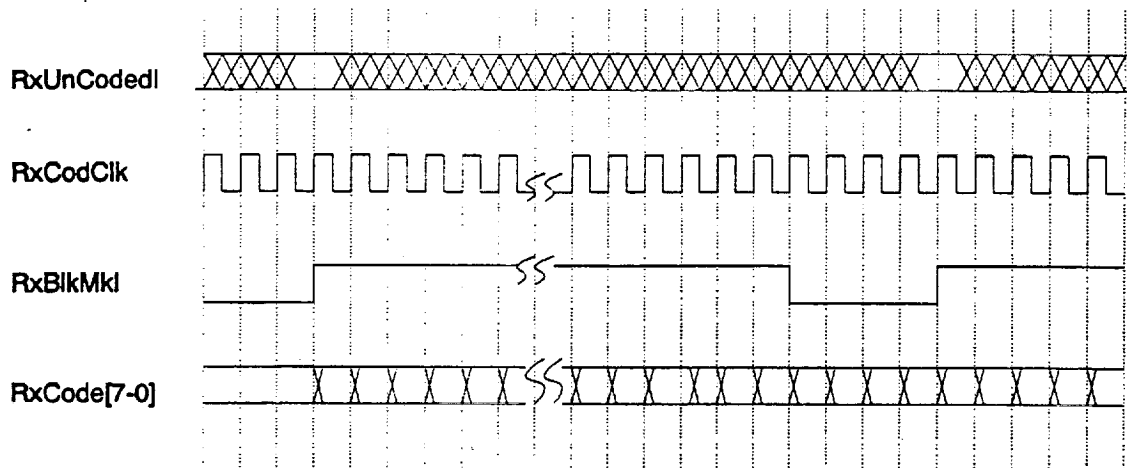
Power Consumption



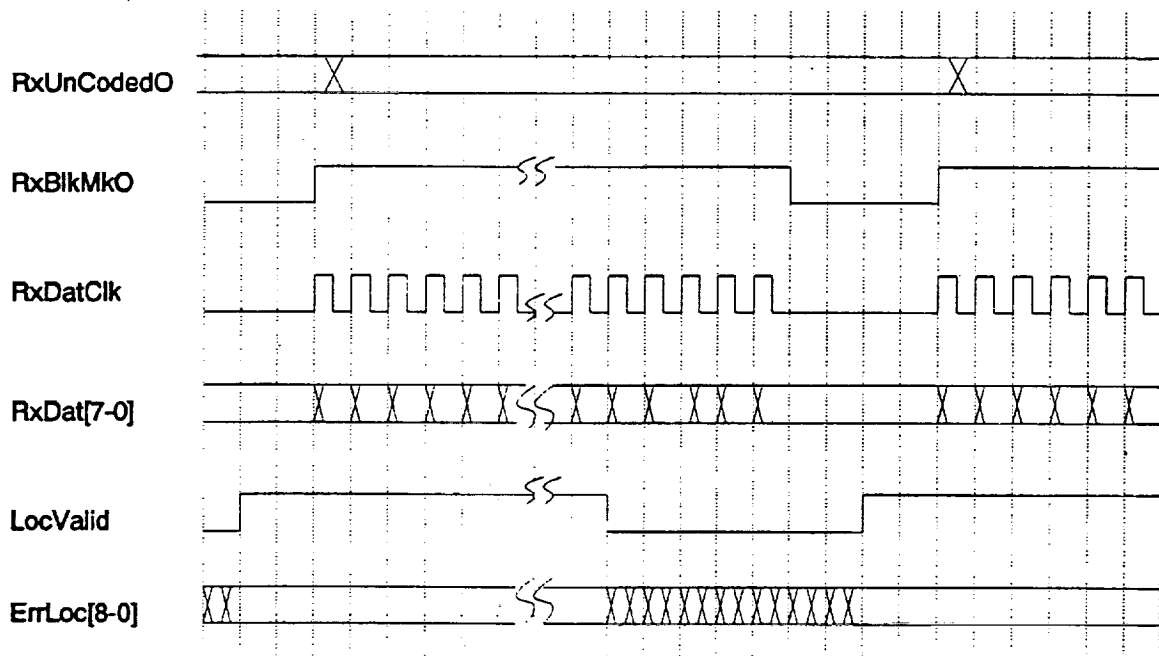
Absolute Maximum Ratings Over Specified Temperature Range	
Condition/Characteristic	Range
Supply voltage range, Vss	-0.3 V to 7.0 V
Input voltage range	-0.3 V to 7.0 V
Output voltage range	-0.3 V to 7.0 V
Continuous power dissipation	-0.3 V to 7.0 V
Operating free air temperature	0°C to 70°C
Storage temperature	-40°C to +125°C

Recommended Operating Conditions				
Operating Condition	Min	Nom	Max	Unit
Supply Voltage Vss	4.75	5.0	5.25	Volts
Vin high	2.0			Volts
Vin low			0.8	Volts
Vout high	2.4			Volts
Vout low			0.5	Volts

Receive Timing In



Receive Timing Out



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